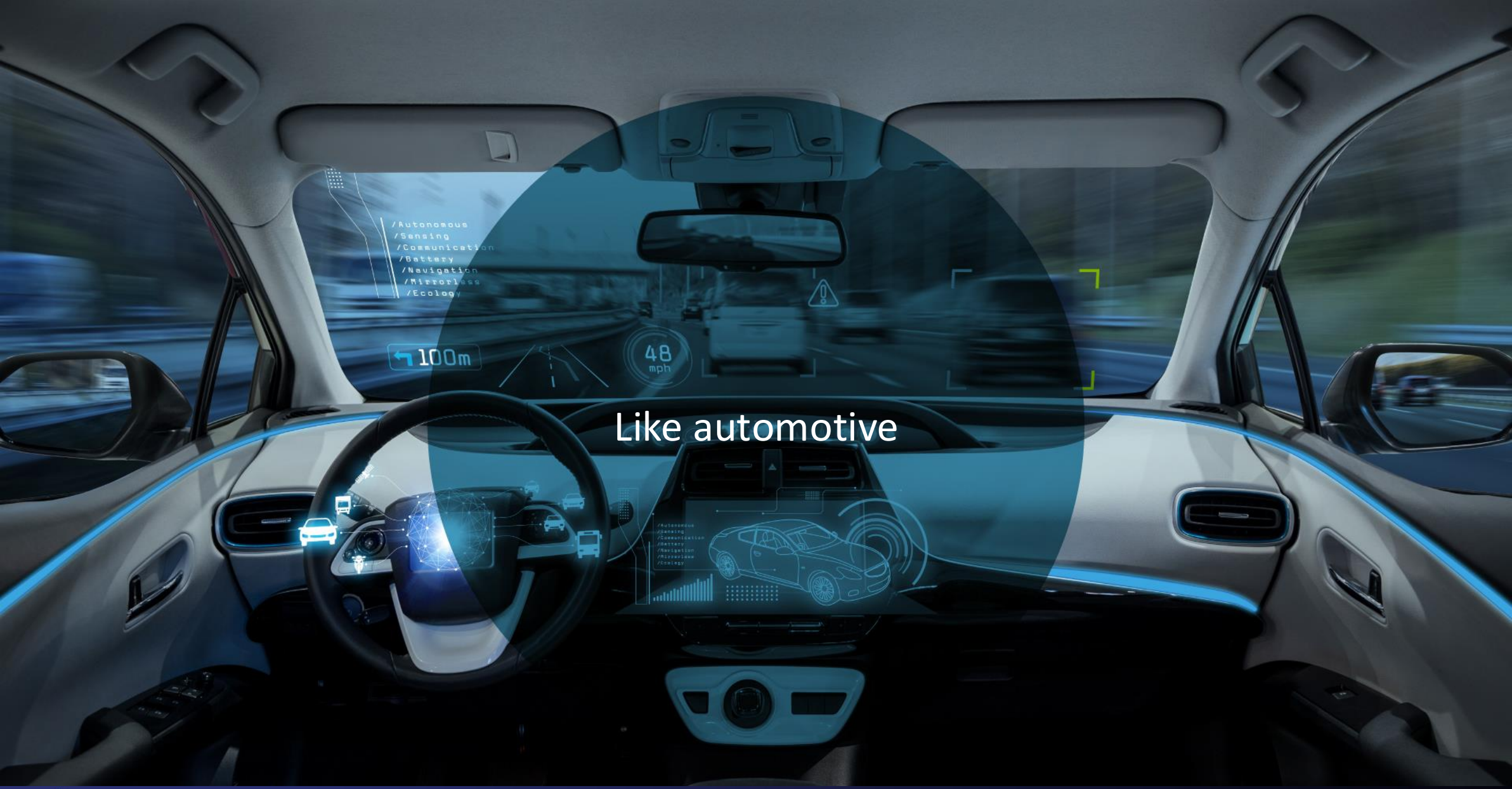
NanoIC: Accelerating beyond-2nm innovation across the ecosystem

Jo De Boeck, EVP and CSO, imec


NanoIC
NanoIC aims to fulfil the European Chips Act's vision for leadership and competitiveness in advanced system-on-chip innovation.

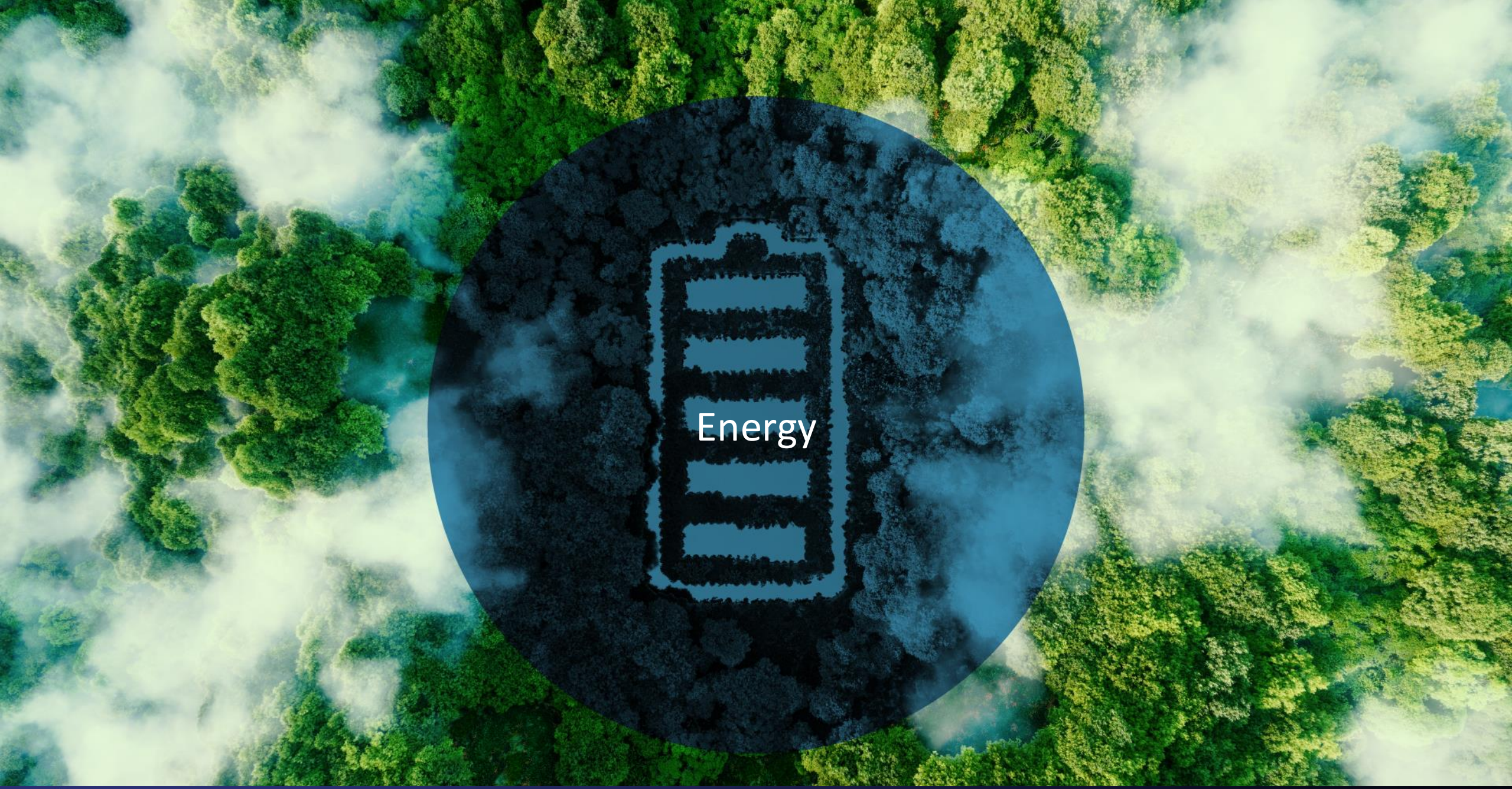

Critical markets requiring high integration and efficiency will be strongly impacted by these technologies.



Like automotive


Consumer electronics


AR/VR


Energy


Health

The NanoIC pilot line is hosted and coordinated by

imec

and leverages existing and new tools in its fabs

NanoIC

Pilot line project partners

imec | cea leti | Fraunhofer MIKROELEKTRONIK | Tyndall National Institute Institiúid Náisiúnta | VTT | University Politehnica of Bucharest 205 Years of Innovation 1818

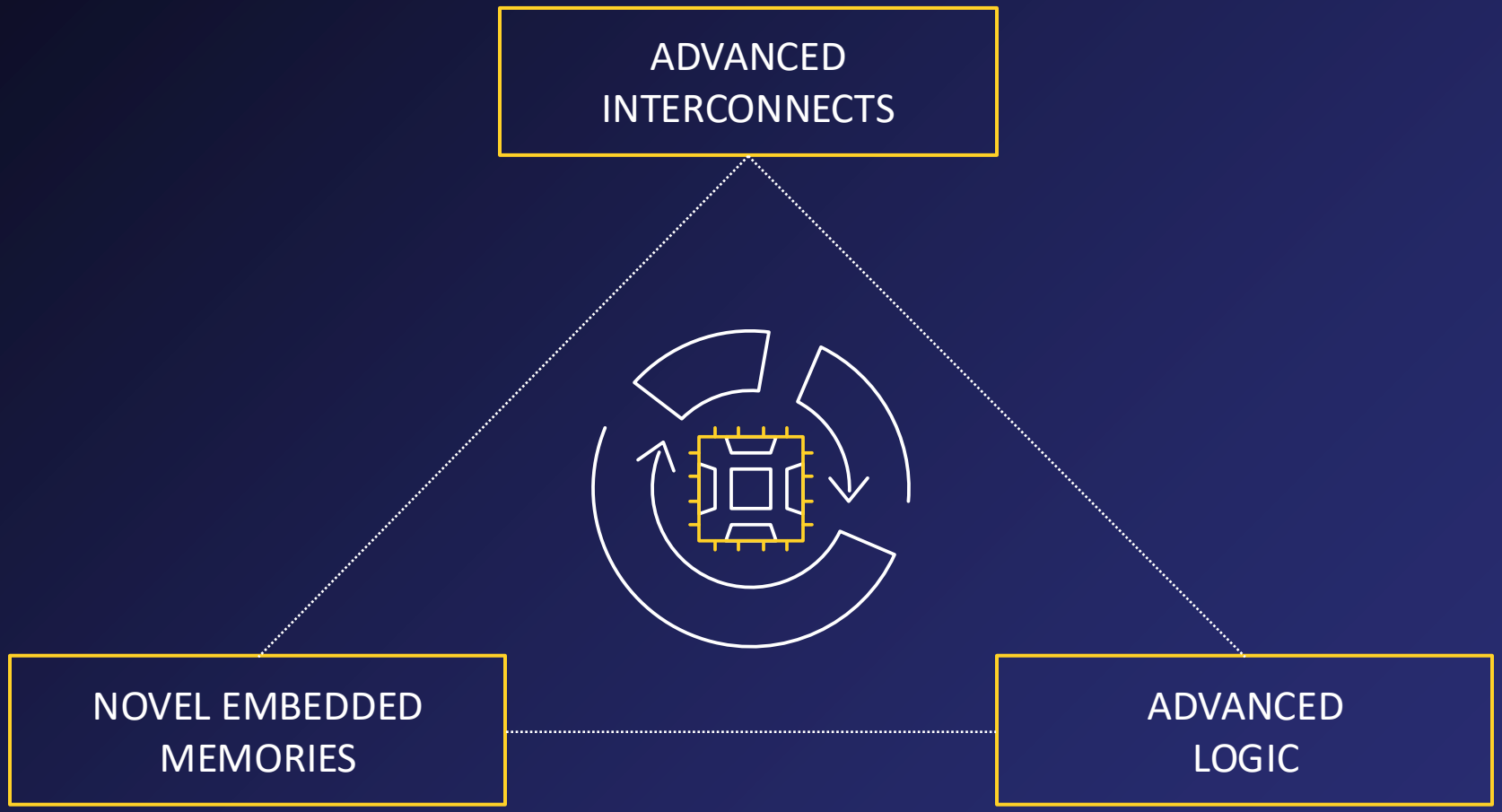
Coordinated by imec

Supported by Vlaamse overheid

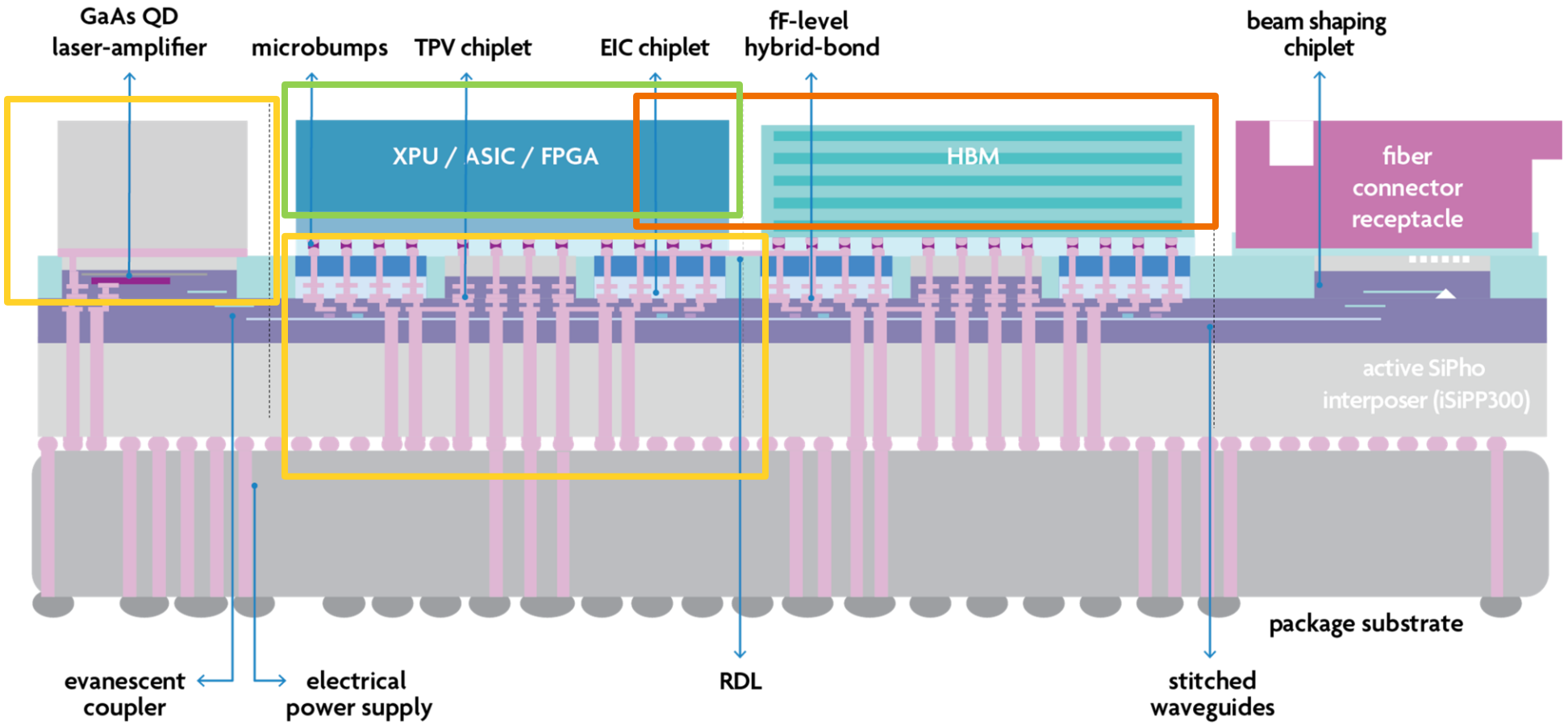
Co-funded by Chips JU

Rendering of the NanoIC pilot line, an extension of imec's facilities.

To enable beyond 2nm SoC, the NanoIC pilot line offers collaborative R&D possibilities:

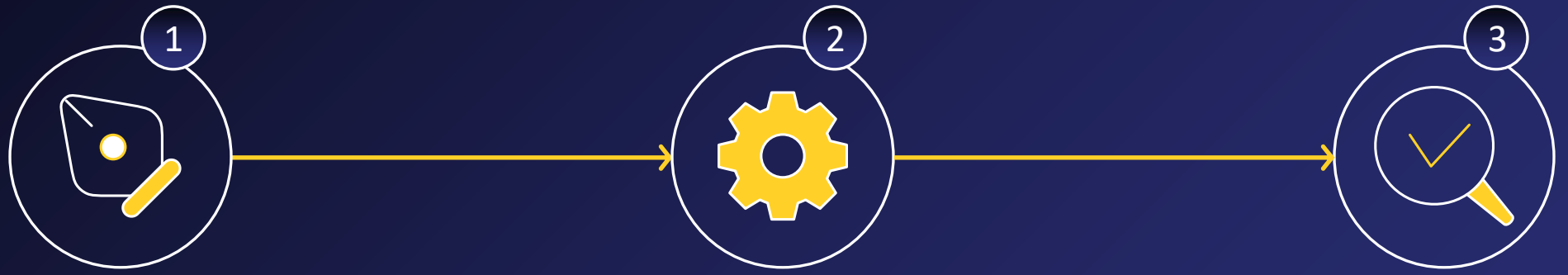


Example of a future compute system



Advanced interconnects | Novel memories | Advanced logic

How to access NanoIC



Design

Access through PDK

Process

Baseline processes & module set-up at higher TRL level

Demonstrators

Validation of new capability/infrastructure

To enable the exploration of the potential impact of the pilot line technologies, NanoIC will offer:

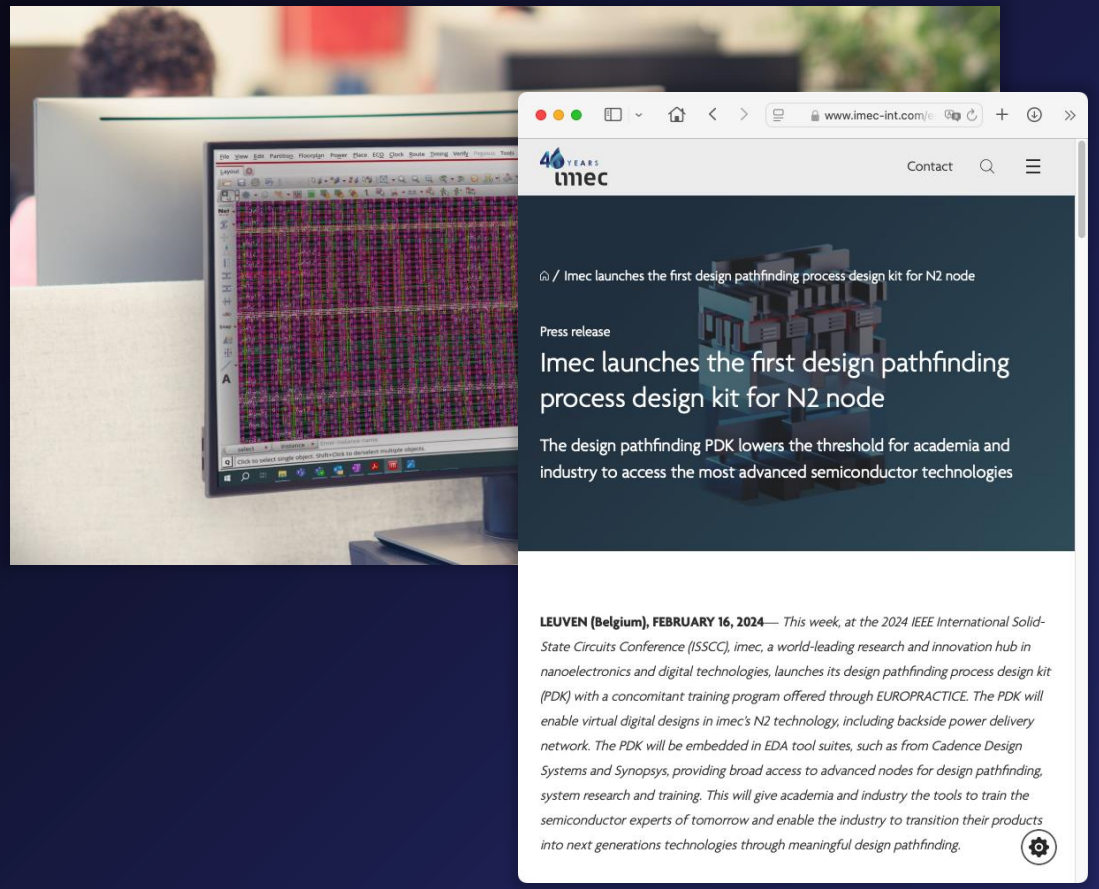
DESIGN PATHFINDING
PDKs

SYSTEM EXPLORATION
PDKs

available to academia and designers
(including SMEs and start-ups)

N2 design pathfinding PDK already available

Launched in February 2024



Two training sessions: June and Dec. 2024

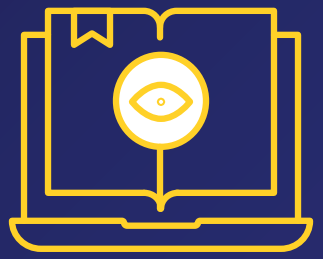
Follow us on LinkedIn for trainings in 2025!

To build a skilled European semiconductor workforce, the NanoIC pilot line offers:

Opportunities for **PhD** students and **internships**

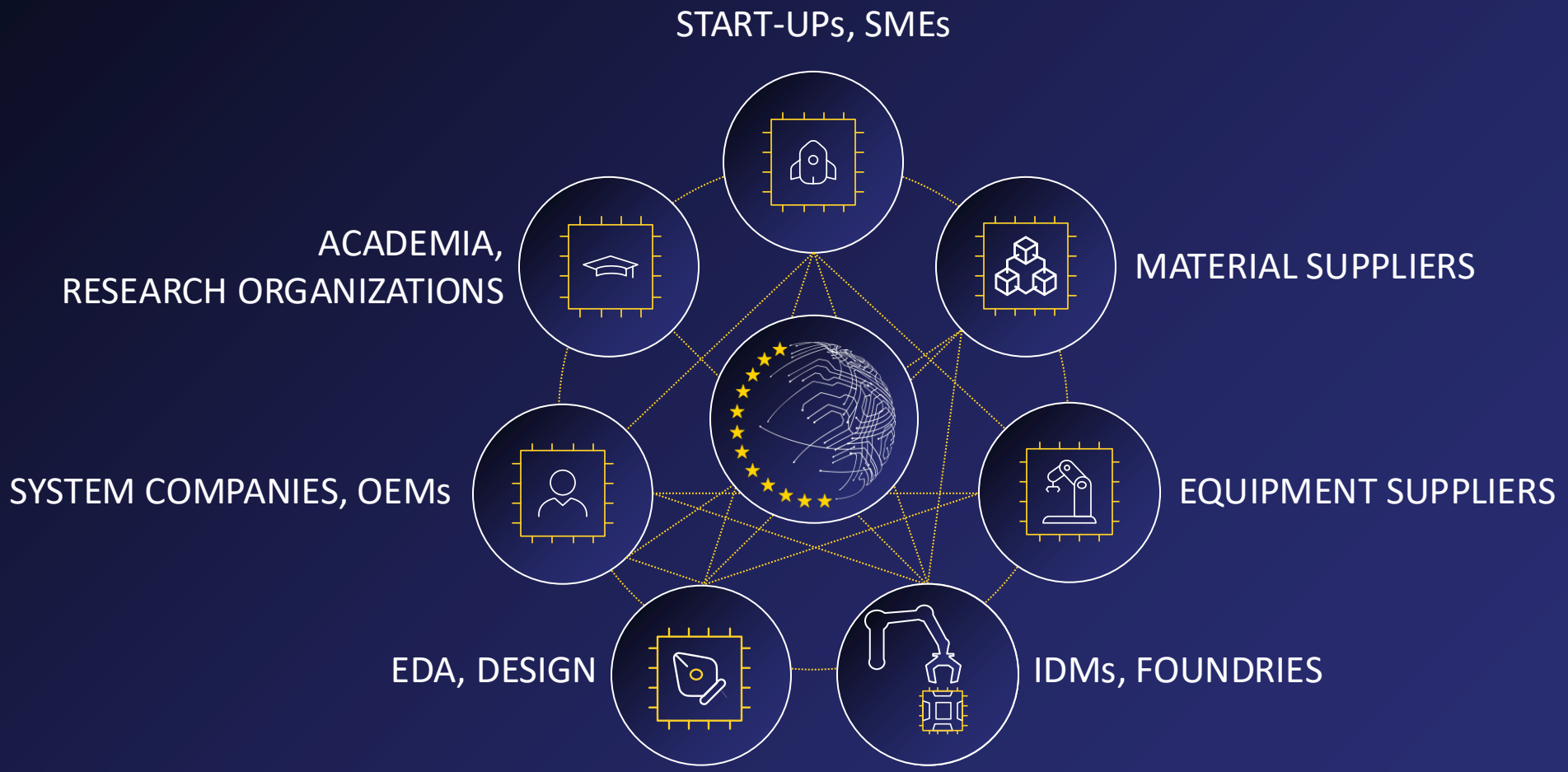
PDK workshops

Bootcamps



Expert courses

The NanoIC pilot line offers opportunities for the entire ecosystem:



NanoIC's below-2nm objective on imec's logic technology roadmap

2018	2020	2023	2025	2027	2029	2031	2033	2035	2037	2039
N7	N5	N3	N2	A14	A10	A7	A5	A3	A2	sub-A2

DEVICE AND MATERIAL INNOVATIONS

	FinFET			NanoSheet			CFET			2DFET, ?, …	
	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled
Metal Tracks	6	6	6	5	5	5	4	<4	<4	<4	<4

CONTINUED DIMENSIONAL SCALING

		0.33NA EUV			0.55NA EUV				0.75NA EUV ?		
Metal Pitch [nm]	40	28	23	22	21	18	18-16	18-14	16-12	16-12	14-10

CHIP INTERCONNECT ARCHITECTURE

				Back-side Power - Global interconnects			Back-side Power - Local signal lines				
Back-side Metal Pitch estimate [nm]		-	-	160-65	115-45	90-42	40-34	40-28	tbd	tbd	…

Join the NanoIC journey…

.. by collaborating and gaining access to cutting-edge chip technologies and engaging in pre-competitive joint R&D...


… by participating in our internships, expert courses, and workshops set to build a skilled semiconductor workforce.

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The acquisition and operation of the Chips JU pilot line is funded jointly by the Chips Joint Undertaking, through the European Union's Digital Europe programme and Horizon Europe programme, as well as by the participating states: Flanders, France, Germany, Ireland, Finland and Romania.

Discover more on
nanoic-project.eu

And follow us
on LinkedIn!